



STV160NF03L

N - CHANNEL 30V - 0.0019Ω - 160A PowerSO-10 STripFET™ MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STV160NF03L	30 V	< 0.0028 Ω	160 A

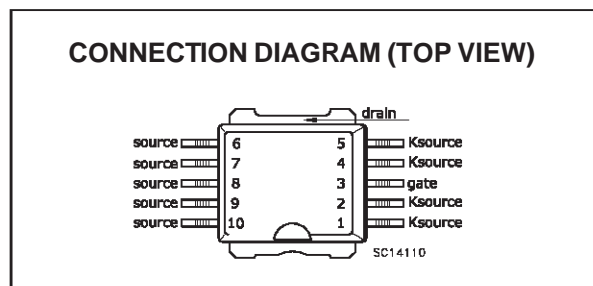
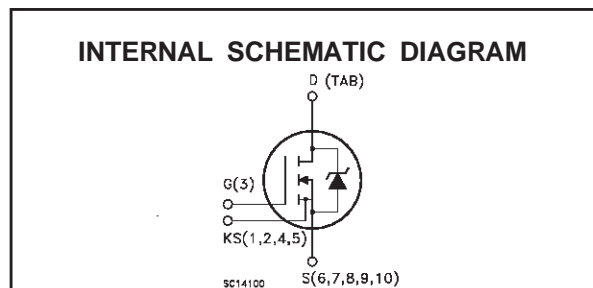
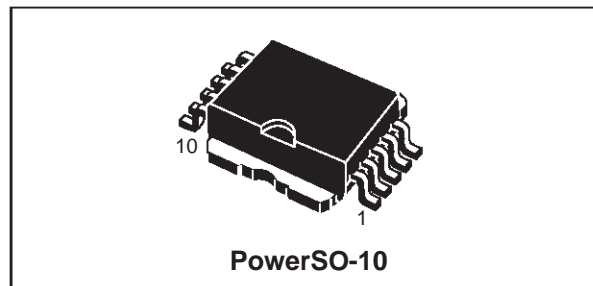
- TYPICAL R_{DS(on)} = 0.0019 Ω
- ULTRA LOW ON-RESISTANCE
- ULTRA FAST SWITCHING
- 100% AVALANCHE TESTED
- VERY LOW GATE CHARGE
- LOW THRESHOLD DRIVE
- LOW PROFILE, VERY LOW PARASITIC INDUCTANCE PowerSO-10 PACKAGE

DESCRIPTION

The **STV160NF03L** represents the second generation of Application Specific STMicroelectronics well established STripFET™ process based on a very unique strip layout design. The resulting MOSFET shows unrivalled high packing density with ultra low on-resistance and superior switching characteristics. Process simplification also translates into improved manufacturing reproducibility. This device is particularly suitable for high current, low voltage switching application where efficiency is crucial.

APPLICATIONS

- BUCK CONVERTERS IN HIGH PERFORMANCE TELECOM AND VRMs DC-DC CONVERTERS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	30	V
V _{GS}	Gate-source Voltage	± 20	V
I _D (**)	Drain Current (continuous) at T _c = 25 °C	160	A
I _D	Drain Current (continuous) at T _c = 100 °C	113	A
I _{DM} (•)	Drain Current (pulsed)	640	A
P _{tot}	Total Dissipation at T _c = 25 °C	160	W
	Derating Factor	1.07	W/°C
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

(**) Limited only maximum junction temperature allowed by PowerSO-10

STV160NF03L

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.9375	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	50	$^{\circ}C/W$
T_I	Maximum Lead Temperature For Soldering Purpose		300	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$ $V_{GS} = 0$	30			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 25^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 15 V$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$ $T_c = 25^{\circ}C$	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$ $I_D = 80 A$ $V_{GS} = 8V$ $I_D = 80 A$ $V_{GS} = 4.5V$ $I_D = 40 A$ $V_{GS} = 10V$ $I_D = 80 A$ $T_j = 175^{\circ}C$ $V_{GS} = 8V$ $I_D = 80 A$ $T_j = 175^{\circ}C$ $V_{GS} = 4.5V$ $I_D = 40 A$ $T_j = 175^{\circ}C$		1.9 2.0 4.0	2.8 3.8 6.7 6.4 7.8 12.8	$m\Omega$ $m\Omega$ $m\Omega$ $m\Omega$ $m\Omega$ $m\Omega$
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	160			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 80 A$		210		S
R_g	Gate resistance	$V_{DS} = 15 V$ $f = 1 MHz$ $V_{GS} = 0$		0.9		Ω
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 15 V$ $f = 1 MHz$ $V_{GS} = 0$		4900 2950 565		pF pF pF
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 0 V$ $f = 1 MHz$ $V_{GS} = 0$		7200 13000 4220		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 40\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, see fig. 3)		23		ns
t_r	Rise Time			350		ns
Q_g	Total Gate Charge	$V_{DD} = 16\text{ V}$ $I_D = 160\text{ A}$ $V_{GS} = 10\text{ V}$		103		nC
Q_{gs}	Gate-Source Charge			38		nC
Q_{gd}	Gate-Drain Charge			9		nC

SWITCHING OFF

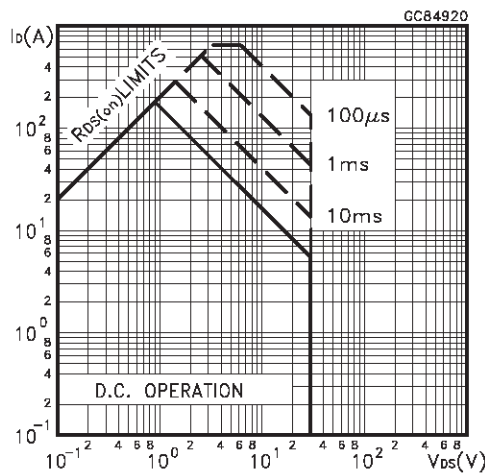
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 40\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, see fig. 3)		105		ns
t_f	Fall Time			120		ns
$t_{d(off)}$	Turn-off Delay Time	$V_{clamp} = 16\text{ V}$ $I_D = 80\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Inductive Load, see fig. 5)		85		ns
$t_{r(Voff)}$	Off-voltage Rise Time			46		ns
t_f	Fall Time			335		ns
t_c	Cross-over Time			404		ns

SOURCE DRAIN DIODE

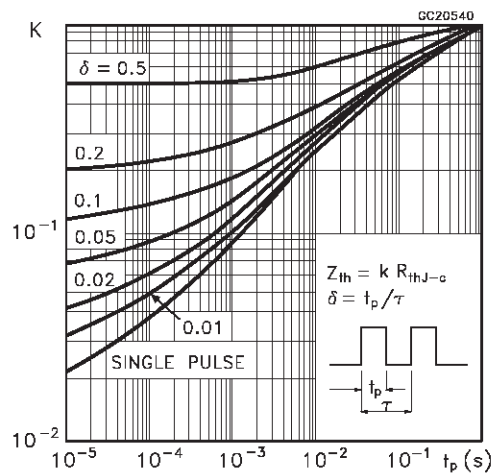
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				160	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				640	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 160\text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 80\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ (see test circuit, fig. 5)		100		ns
Q_{rr}	Reverse Recovery Charge			0.25		μC
I_{RRM}	Reverse Recovery Current			5		A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %
 (•) Pulse width limited by safe operating area

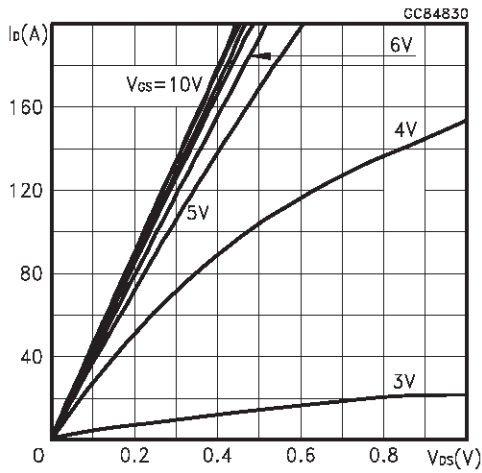
Safe Operating Area



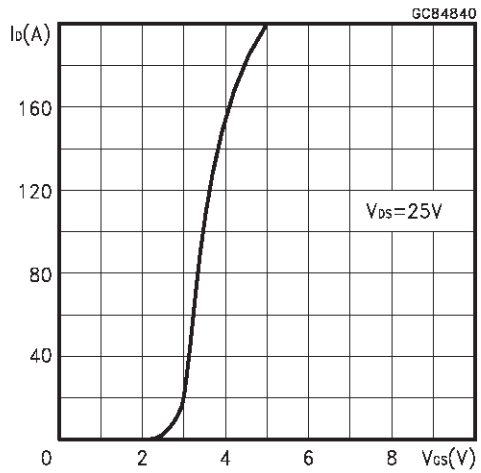
Thermal Impedance



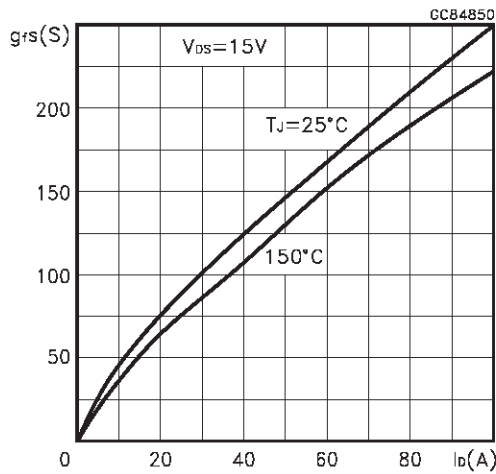
Output Characteristics



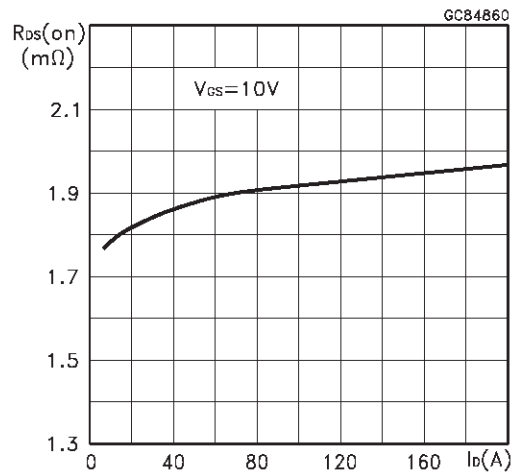
Transfer Characteristics



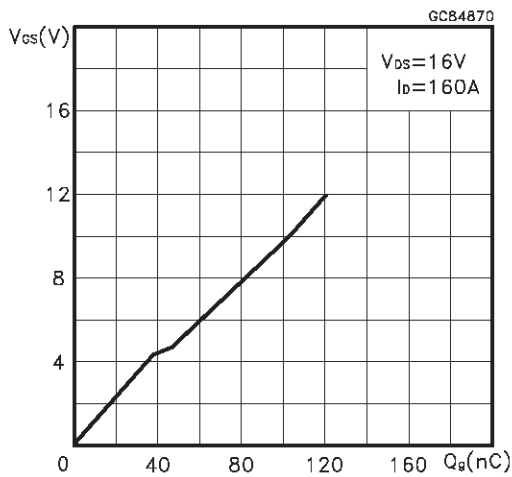
Transconductance



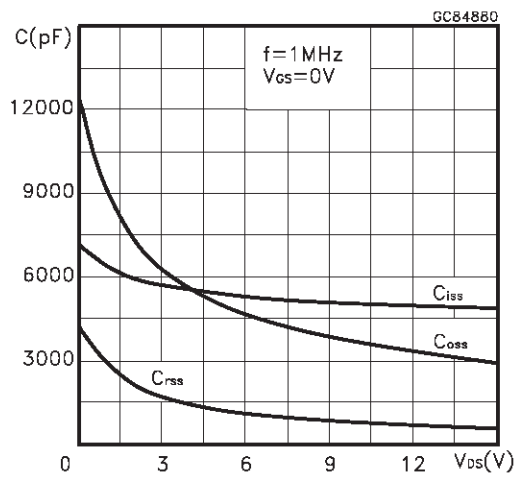
Static Drain-source On Resistance



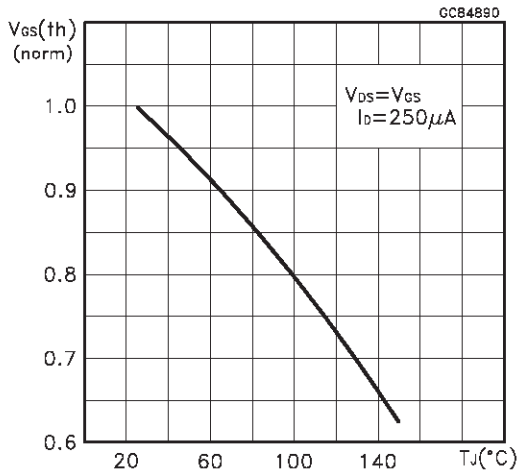
Gate Charge vs Gate-source Voltage



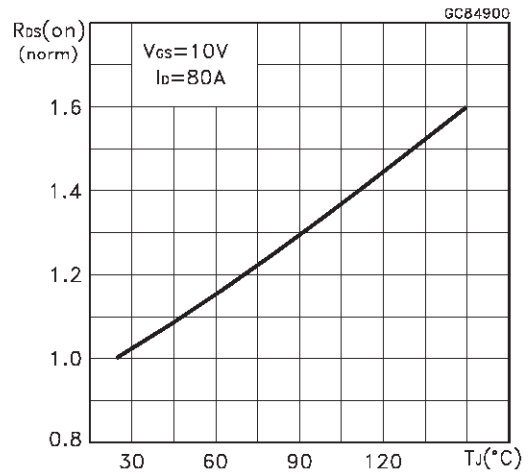
Capacitance Variations



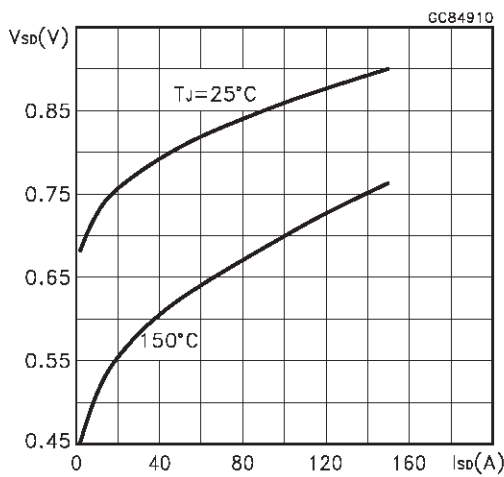
Normalized Gate Threshold Voltage vs Temperature



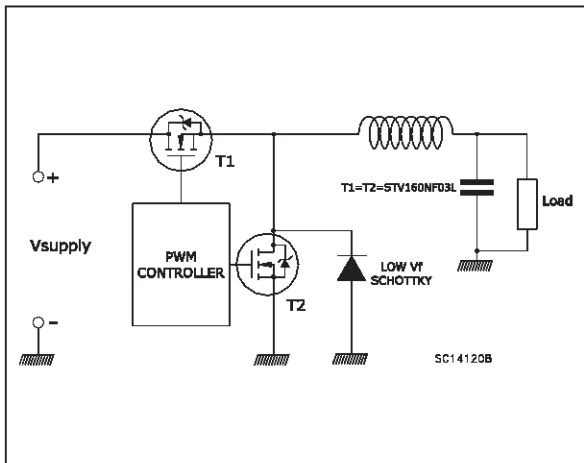
Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Basic Schematic For Motherboard VRM With Synchronous Rectification



Basic Schematic Mosfet Switch Used In Secondary Side Of a Foward Convert

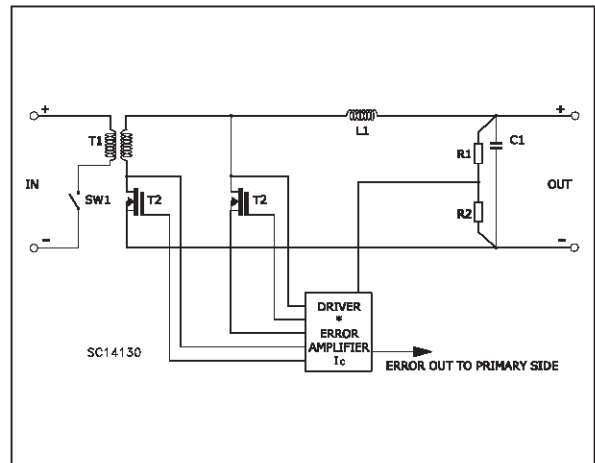


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform

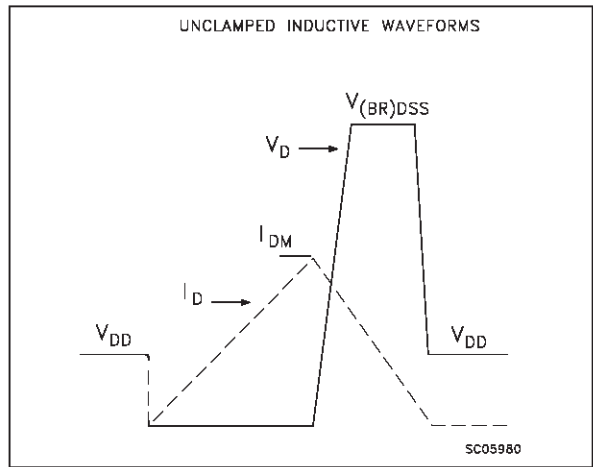


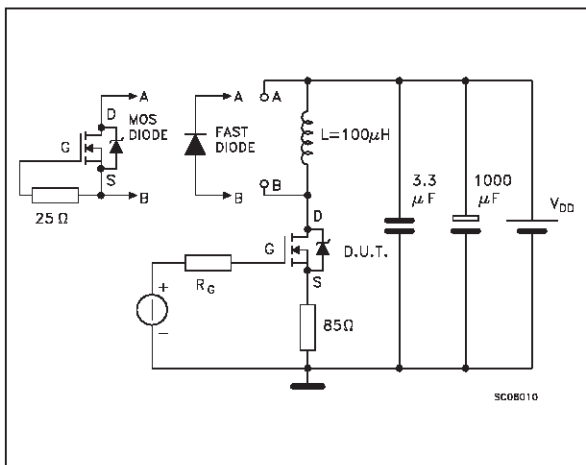
Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Gate Charge test Circuit

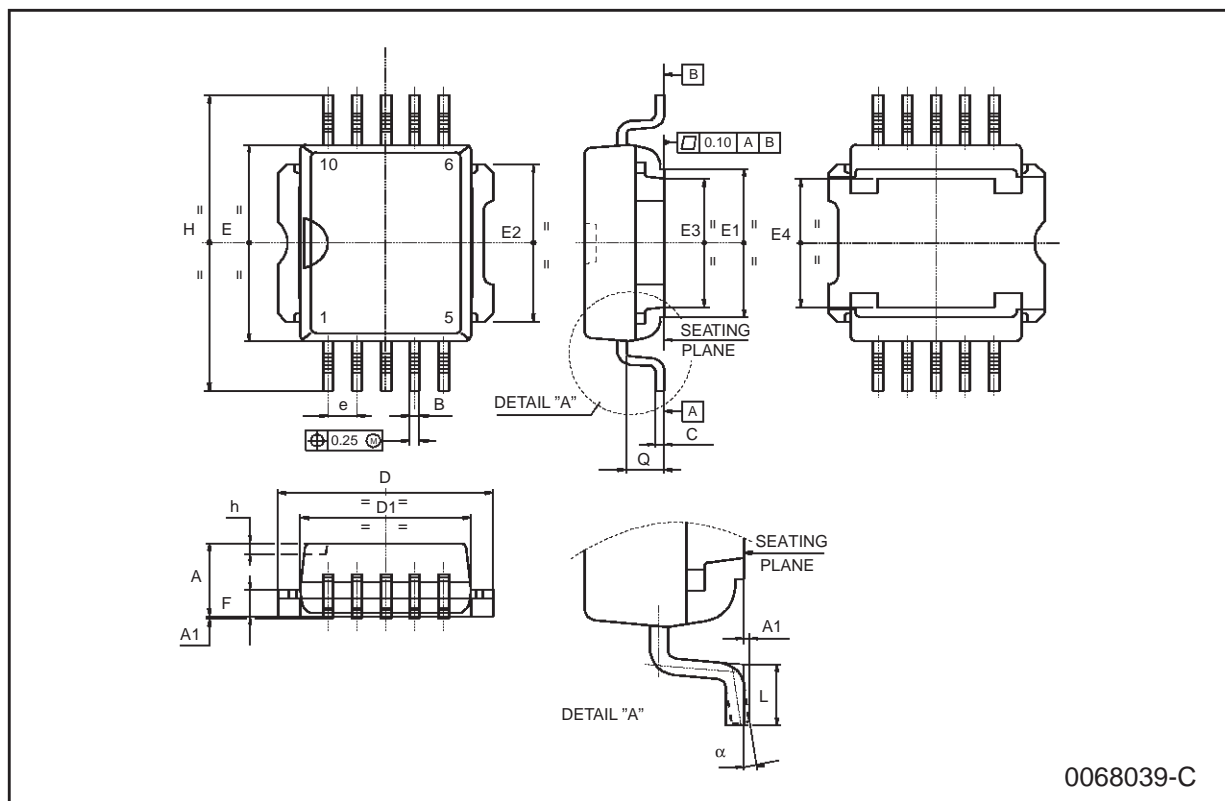


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



PowerSO-10 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0°		8°			



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1999 STMicroelectronics – Printed in Italy – All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.